ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor memory cell structure and method of manufacture. The method includes the steps of forming a shallow first-type well layer, a second-type well layer and a deep first-type well layer over a substrate, forming stack gates over the shallow first-type well layer and finally forming source terminals and drain terminals. The source terminals penetrate through the shallow first-type well layer and connect with the second-type well layer. The drain terminals are close to the surface of the shallow first-type well layer. Both the source terminals and the drain terminals contain second type dopants.